JAYNARAYAN THAKURDAS TUDU

Dept of Computer Science and Engineering
Indian Institute of Technology Tirupati
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RESEARCH INTEREST

Design for Test of VLSI Circuits, Computer Aided Design, Fault Tolerant and Reliable Architecture, Power Aware Computer Architecture, Hardware verification, and Post-silicon Debug.

TEACHING INTEREST

Basic Digital Designs, Programming in C/C++, Computer Architecture, Microprocessor Design, Data Structure and Algorithm, Computer Aided Design of VLSI, Test and Verification of VLSI Design, and Advanced Topics in Low Power Testing.

EDUCATION

PhD in Computer Science, Indian Institute of Science, Bangalore,
CGPA: 7.5/10, July, 2010 - July, 2017 (Submitted in July 2016 and Awarded in July 2017).
Major Courses: Linear Algebra, Algorithm and Analysis, Graph Theory, Embedded System, CMOS VLSI, and CAD for VLSI.
Thesis: Power Issues in SoC: Power Aware DFT Architecture and Power Estimation.

MSc (Engg) in Computer Science, Indian Institute of Science, Bangalore,
CGPA: 7.5/10, Aug, 2007 - July, 2010.
Major Courses: Computer Architecture, Operating System, Modelling and Simulation, Processor Design, and Test & Verification of SoC.
Thesis: Low Power Test Methodology for SoC: Solutions for Peak Power Minimization.

BE in Computer Science and Engineering, Institute of Technical Education and Research, Bhubaneswar,
Percentage: 63.00%, Sept, 2001 - Nov, 2005.
Major Courses: Digital Electronics and Microprocessor, Computer Architecture and Organization, Operating System, Programming Language, Computer Network, Algorithm Design and Analysis.
Project: Online Library Information System Using Visual Basic and Dot Net.

RESEARCH/TEACHING EXPERIENCE

July 2018 - Current: Assistant Professor, Dept. of Computer Science and Engineering
Responsibility: Teaching, Research, and Infrastructure Development

June 2017 - July 2018: Research Scientist, jointly with CADS Lab., Dept. of Electrical Engineering and Gigabits Networking Lab, Dept. of Computer Sci and Engg, IIT Bombay
(worked with Prof. Virendra Singh and Prof. Ashwin Gumaste)

Feb 2017 - May 2017: Lab Engineer at VLSI Circuit and System Laboratory,
ECE, IISc Bangalore
(worked with Prof. Bharadwaj Amrutur)
Project: MSP 430 Based Smart Probe Micro-controller for Aircraft.

Sept 2016 - Jan 2017: Research Assistant at CADS Lab, Electrical Engineering, IIT Bombay.
Hosted by Prof. Virendra Singh
Research Problem: Hardware Security: Scan Based Side Channel Attack.

Nov 2014 - June 2015: Research Internship at CADS Lab, EE, IIT Bombay
(worked with Prof. Virendra Singh).
Research Topic: Low Power Design for Test Scan Architecture.

July 2010 - Dec 2011: Internship at LSI Research, India on a collaborative project between LSI Research and SERC, IISc Bangalore, India
Research Problem: Power Issues in Scan Chain during Capture and Shift Operation.

Aug 2006 - July 2007: Lecturer at Silicon Institute of Technology, Bhubaneswar, Odisha
Courses taught: Computer Architecture, Algorithm Design and Programming Language in C/C++

RESEARCH SUMMARY

Thesis

- **PhD:** Power Issues in SoC: Power Aware DFT Architecture and Power Estimation.

  Summary: We study the power problems in System-on-Chip (SoC) designs from the design-for-test (DFT) perspective. In particular, we study two problems: 1) ultra low power DFT architecture and 2) the worst case power estimation. The thesis contribute three major solutions to the problems of interest: 1) Scan chain reordering for peak power minimization, 2) JScan: A new DFT architecture to solve test time, data volume, and test power problems, and 3) Input vector generation for worst power estimation using Integer Linear Programming. Sufficient experiments has been carried out to demonstrate the efficacy of each of the proposed solutions. All the proposed methodology and experimental results are published in the appropriate fora.

  Link: `http://etd.iisc.ac.in/handle/2005/3003`

- **MSc(Engg):** Low Power Test Methodology for SoC: Solutions for Peak Power Minimization.

  Summary: We investigate the power issues in serial scan DFT based SoC designs. Particularly, we study the peak power issues in the shift and test cycles of the scan operation. Test pattern reordering, scan chain restitching, and test scheduling on SoC modules methodologies are proposed. Experiments are performed on ISCAS 85/89 and ITC 99 circuits for each proposed solutions. All the proposed solutions and experimental results are published in the peer reviewed conferences and journals.

  Link: `http://etd.iisc.ernet.in/handle/2005/2242`

PUBLICATIONS

In Peer reviewed Journals (includes Preprints and Drafts):

1. **Jaynarayan Tudu**, Satyadev Ahlawat, Virendra Singh, "An Architectural Framework for Configurable Design-for-Test (DfT) Architecture". [Status: submitted to IEEE Transaction on VLSI Design, Ref No: TVLSI-00165-2019].
2. Satyadev Ahlawat, **Jaynarayan Tudu**, Anzhela Matrosova, Virendra Singh, "A High Performance Scan Flip-Flop Design for Serial and Mixed Mode Scan Test", IEEE Transaction on Device and Materials Reliability, Vol. 18 (2), 2018.

In Peer reviewed Conferences:

1. Satyadev Ahlawat, Kailash Ahirwar, **Jaynarayan Tudu**, Masahiro Fujita, Virendra Sing, Securing Scan through Plain-text Restriction, Proc of 25^{th} IEEE Intl Symposium on Online Testing and Robust System Design (IOLTS-19), Rhodes Island, Greece.[Status: accepted]
2. Darshit Vaghani, Satyadev Ahlawat, **Jaynarayan Tudu**, Masahiro Fujita, and Virendra Singh, "On Securing Scan Design Through Test Vector Encryption", Accepted to be published in IEEE International Symposium on Circuits and Systems (ISCAS) 2018, Florence, Italy, May 27-30, 2018. DOI: TBA.
3. Satyadev Ahlawat, Darshit Vaghani, **Jaynarayan Tudu**, and Ashok Suhag, "A Cost Effective Technique for Diagnosis of SCan Chain Faults", *Proceedings of 21^{st} International Symposium on VLSI Design and Test (VDAT 2017)*, Roorkee, India, June 29 - July 2, 2017. Communication in Computer and Information Science, Vol 711, Springer, Singapore, pp. 191-204. DOI: https://doi.org/10.1007/978-981-10-7470-7_20.
4. Binod Kumar, Ankit Jindal, **Jaynarayan Tudu**, Brajesh Pandey, Virendra Singh, "Revising Random Access Scan for Effective Enhancement of Post-silicon Observability", *23^{rd} IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS)*, Thessaloniki, Greece, July 3-5, 2017, pp. 132-137. DOI: https://doi.org/10.1109/IOLTS.2017.8046208.
5. Satyadev Ahlawat, Darshit Vaghani, **Jaynarayan Tudu**, Virendra Singh, "On Securing Scan Design from Scan-Based Side-Channel Attacks", Accepted to be published in *Proceedings of 26^{th} IEEE Asian Test Symposium (ATS)*, 2017, Taipei, Taiwan, November 27-30, 2017. DOI: TBA.
6. Binod Kumar, Ankit Jindal, Boda Nehru, Brajesh Pandey, **Jaynarayan Tudu** and Virendra Singh, "A Technique for Low Power, Stuck-at Fault Diagnosable and Reconfigurable Scan Architecture", *IEEE East-West Design & Test Symposium (EWDTS) 2016*, Yerevan, Armenia, October 14-17, 2016. DOI:http://doi.org/10.1109/EWDTS.2016.7807675.
7. Satyadev Ahlawat, **Jaynarayan Tudu**, Anzhela Matrosova, and Virendra Singh, "A High Performance Scan Flip-Flop Design for Serial and Mixed Mode Scan Test", *Proc. IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS) 2016*, Catalunya, Spain, 4-6 July, 2016, pp. 233-238 DOI: https://doi.org/10.1109/IOLTS.2016.7604709.
8. **Jaynarayan Tudu**, "JSCAN: A Joint-scan DFT Architecture to Minimize Test Time, Data Volume, and Test Power", *Proceedings 20^{th} IEEE International Symposium on VLSI Design and Test (VDAT) 2016*, Guwahati, India, May 24-27, 2016. DOI:https://doi.org/10.1109/ISVDAT.2016.8064866.
9. **Jaynarayan Tudu** and Satyadev Ahlawat, "Guided Shifting of Test Pattern to Minimize Test Time in Serial Scan", *Proceedings 20^{th} IEEE International Symposium on VLSI Design and Test (VDAT) 2016*, Guwahati, India, May 24-27, 2016. DOI:https://doi.org/10.1109/ISVDAT.2016.8064851.
10. Satyadev Ahlawat and **Jaynarayan Tudu**, "On Minimization of Test Power through Modified Scan Flip-flop", *Proceedings 20^{th} IEEE International Symposium on VLSI Design and Test (VDAT) 2016*, Guwahati, India, May 24-27, 2016. DOI:https://doi.org/10.1109/ISVDAT.2016.8064878.
11. Binod Kumar, Boda Nehru, Brajesh Pandey, and **Jaynarayan Tudu**, "Skip-scan: A Methodology for Test Time Reduction", *Proceedings 20^{th} IEEE International Symposium on VLSI Design and Test (VDAT) 2016*, Guwahati, India, May 24-27, 2016. DOI:https://doi.org/10.1109/ISVDAT.2016.8064869.
12. Rohin Gulve, Nihar Hage, and **Jaynarayan Tudu**, "On Determination of Instantaneous Peak and Cycle Peak Switching using ILP", *Proceedings 20^{th} IEEE International Symposium on VLSI Design and Test (VDAT) 2016*, Guwahati, India, May 24-27, 2016. DOI:https://doi.org/10.1109/ISVDAT.2016.8064881.
13. Satyadev Ahlawat, **Jaynarayan Tudu**, Anzhela Matrosava, Virendra Singh, "A New Scan Flip Flop Design to Eliminate Performance Penalty of Scan", 24^{th} *IEEE Asian Test Symposium (ATS) 2015*, Mumbai, India, Nov 22-25, 2015. DOI: https://doi.org/10.1109/ATS.2015.12.

14. **Jaynarayan Tudu**, Deepak Malani, Virendra Singh, "Level-Accurate Peak Activity Estimation in Combinational Circuit Using BILP", *Proceeding in* 17^{th} *International Symposium on VLSI Design and Test(VDAT), 2013*, Jaipur, India. Communication in Computer and Information Science, Springer, Vol. 382, pp. 345-352. DOI: `https://doi.org/10.1007/978-3-642-42024-5_41`.
15. **Jaynarayan Tudu**, Deepak Malani, and Virendra Singh, "ILP Based Approach for Input Vector Controlled Toggle Maximization in Combinational Circuits", 16^{th} *International Symposium on VLSI Design and Test (VDAT) 2012*, Kolkata, India, July 2012. Lecture Notes in Computer Science, vol 7373, Springer, Berlin, Heidelberg, pp. 172-179. DOI:`https://doi.org/10.1007/978-3-642-31494-0_20`.
16. **Jaynarayan Tudu**, Erik Larsson, Virendra Singh, and Hideo Fujiwara, "Scan Cell Reordering to Minimize Peak Power During Test Cycle: A Graph-theoretic Approach", 15^{th} *IEEE European Test Symposium (ETS) 2010*, Prague, Czech Rep., May 24-28, 2010. DOI:`https://doi.org/10.1109/ETSYM.2010.5512732`.
17. **Jaynarayan Tudu**, Erik Larsson, Virendra Singh, and Hideo Fujiwara, "Graph-theoretic Approach for Scan Cell Reordering to Minimize Peak Shift Power", 20^{th} *ACM Great Lake Symposium on VLSI (GLSVLSI) 2010*, Providence, Rhode Island, USA, May 16-18, 2010. DOI:`https://doi.org/10.1145/1785481.1785499`.
18. **Jaynarayan Tudu**, Erik Larsson, Virendra Singh, and Adit Singh, "Capture Power Reduction for Modular System-on-Chip Test", *IEEE/VSI VLSI Design and Test Symposium (VDAT)*, Bangalore, India, July, 2009. DOI: Not available.
19. **Jaynarayan Tudu**, Erik Larsson, Virendra Singh, and Vishwani D. Agrawal, "On Minimization of Peak Power during SoC Test", 14^{th} *IEEE European Test Symposium (ETS) 2009*, Seville, Spain, May 24-29, 2009. DOI: `https://doi.org/10.1109/ETS.2009.36`.
20. Pramod Subramanyan, Ram Rakesh Jangir, **Jaynarayan Tudu**, Erik Larsson, and Virendra Singh, "Generation of Minimum Leakage Input Vectors with Constrained NBTI Degradation",*IEEE East-West Design and Test Symposium (EWDTS) 2009*, Moscow, Russia, September 2009. DOI: Not Available.

In Peer reviewed Workshops:

1. Binod Kumar, Ankit Jindal, **Jaynarayan Tudu**, and Brajesh Pandey, "An Integrated solution for manufacturing testing and post silicon validation", 8th IEEE International Workshop on Reliability Aware System Design and Test (RASDAT) 2017, Hyderabad, Jan 2017.
2. Binod Kumar, Ankit Jindal, **Jaynarayan Tudu** and Virendra Singh, "A Methodology For Post-Silicon Debug Utilizing Progressive Random Access Scan Architecture", *The Seventeenth IEEE Workshop on RTL and High Level Testing (WRTLT) 2016*, Hiroshima, Japan, November 24-25, 2016.
3. **Jaynarayan Tudu** and Virendra Singh, "Guided shifting of test patterns to minimize the test time in serial scan," 15th IEEE Workshop on RTL and High Level Testing (WRTLT14) 2014, Hangzhou, China, Nov 2014.
4. Satdev Ahlawat, **Jaynarayan Tudu**, Virendra Singh, Shashidhar Bapat, and Karthik Madhugiri, "Low power scan flip-flop design to eliminate output gating overhead for critical paths", IEEE International Workshop on Reliability Aware System Design and Test (RASDAT) 2012, Hyderabad, India, Jan 2012.
5. Satdev Ahlawat, Ashok Suhag, **Jaynarayan Tudu**, and Virendra Singh, "Power aware scan flip-flop design for scan test", 13th IEEE Workshop on RTL and High Level testing (WRTLT) 2012, Niigata, Japan, Nov 2012.
6. **Jaynarayan Tudu**, Erik Larsson, and Virendra Singh, "Test Scheduling of Modular System-on-chip Under Capture Power Constraints", *11th IEEE Workshop on RTL and High Level Test (WRTLT) 2010*, Shanghai, China, December 2010.

7. **Jaynarayan Tudu**, Erik Larsson, Virendra Singh, and Hideo Fujiwara, "Scan Cells Reordering to Minimize Peak Power during Scan Testing of SoC", IEEE WRTLT 09, Hong Kong, Nov. 2009.

TALKS

- [Conference presentation] "JSCAN: A Joint-scan DFT Architecture to Minimize Test Time, Data Volume, and Test Power", Intnl Symposium on VLSI Design and Test - 2016, IIT Guwahati.
- [Conference presentation] "Guided Shifting of Test Pattern to Minimize Test Time in Serial Scan", Intnl Symposium on VLSI Design and Test - 2016, IIT Guwahati.
- [Workshop presentation] "Scan Cells Reordering to Minimize Peak Power during Scan Testing of SoC", Workshop on RTL and High Level Testing, Nov 2009, Hong Kong University of Sci. and Technology, Hong Kong.
- [Thesis Defence] "Power Issues in SoC: Low Power DFT Architecture and Power Estimation", July 2017, Indian Institute of Science Bangalore, India.
- [Thesis Defence] "Low Power Test Methodology for SoC: Solutions for Peak Power Minimization", May 2010, Indian Institute of Science Bangalore, India.
- [Department talks] Presented two talks on "Low Power Test Issues" at Dept. of Computer Sci. and Automation, Indian Institute of Science, Bangalore.
- [Lab Meeting] Presented series of talks in the area of VLSI Testing, Low Power Design and Test, and Future Trends in CMOS VLSI Design at CADS Lab, Dept. Electrical Engineering, IIT Bombay.

PROFESSIONAL ACTIVITIES

Organising member : RASDAT 2010 - 2018, VDAT 2013, VLSID 2014, ATS 2015, WRTLT 2015, VDAT 2017.
Reviewer : Journal of Electronics Testing: Theory and Application, VDAT 2012, 2013, 2019, VLSID 2012, ATS 2014, 2015, WRTLT 2015, EWDTS 2014.
Session chair : VDAT 2017 for a Verification and Debugging Session.

TOOLS/EXPERIMENTAL EXPERIENCE

- **Programming:** C, C++, Verilog and VHDL.
- **Script:** Python, Perl, Tcl and Bash.
- **Operating System:** Linux (CentOS and Ubuntu), Windows.
- **Tools:** Design Compiler, Cadence RC, Conformal LEC, Cadence ETS, DFT Compiler, VCS (Verilog compiled simulator), PrimeTime, TetraMax, Encounter Test, TestKompress, Apache RedHawk, and SoC Encounter.
- **Miscellaneous:** LaTex, gvim, Matlab/Octave, HTML, gnuplot, xfig, CPLEX (ILP solver), SimpleScalar (Superscalar simulator) and VIS (an open source formal verification tool).
- **Tools developed:**
  - **STPRo**: Scan chain and Test pattern reordering tool (coded in C/C++).
  - **JIVN**: Joint-scan insertion in Verilog netlist (coded in Python).

MISCELLANEOUS

- Served as Asst. Secretary for Odia Sansad, Indian Institute of Science, Bangalore (2011 - 2012).
- Served as Asst. Secretary for AISSQ conference series (www.aissq.org) (2010 - 2015).
- Serving as Associate Editor for Science and Spiritual Quest E-Zine, Bhaktivedanta Institute, Bangalore, and Kolkata.
- Secured All India Rank 50 in JEST 2006 and 535 in GATE 2007 (Computer Science).
- Received GARP Travel grant from IISc to participate in the WRTLT 2009 workshop held at Hong Kong University of Science and Technology, Hong Kong.

PERSONAL DETAILS

Date of birth: 10^{th} April, 1983.
Nationality: Indian
Permanent address:
In care of: Shyam Charan Tudu
Vill.- Sanbhundu, Post.- Tiring
Dist.- Mayurbhanj, Odisha, 757053

DECLARATION

I hereby declare that all the information furnished above are true to best of my knowledge.

Jaynarayan Thakurdas Tudu
Place: IIT Tirupati
Date: 6^{th} May, 2019