Computer System Architecture Laboratory (CS5292)

Indian Institute of Technology Tirupati
L-T-P-C: 0-0-3-2

Jaynarayan T Tudu <jtt@iittp.ac.in>

Objective of the course:

To train the students in the practical aspects of computer architecture. The students will get to learn through a set of experiments the behavior of an underlying computer hardware and its interaction with the program.

Course Content:

The course consists of set of experiments which are intended to understand and explore the underlying computer hardware architecture through programming and architecture simulator. The course will rigorously conduct the architectural programming experiments using C/C++ language. Such program shall probe into the hardware architecture of the given system for which they are compiled. The course will also study the advanced architecture by help of the multi-core simulators like Snipper and GEM5. Additionally, the supporting simulator like SimpleScalar, the cache/memory simulator, and power simulator like MacPat will be used.

Laboratory Experiments:

1. Study of code size in RISC (ARM and RISC-V) and CISC (x86_64) instruction set.
2. Performance Evaluation Metrics: Arithmetic Mean, Geometric Mean, and Standard Deviation.
3. Pipeline Processor Architecture: to experiment on the optimal number of pipeline stages.
4. Branch Predictor: to study the impact of branch predictor on performance.
5. Memory architecture: Impact of size, block size and page fault.
6. Cache memory: Study of cache size, levels, associativity.
7. Installation of Snipper, Pin, GEM5, SimpleScalar, MacPat and other tools.
8. Execution of bench mark programs on Sniper with different configuration for single core architecture.
9. Snipper simulation for multi-core architecture using configuration file.
10. Code modification and architecture implementation in Snipper.
11. Experimenting with the power dissipation (with MacPat and Snipper) and its impact on performance. Understanding the energy-delay-product, performance per watt, and Dark-silicon measurement.
12. GPU characterization using GPGPU-sim simulator.

Evaluation:

Continuous Evaluation: 60% (for 12 experiments).
Continuous evaluation consists of on-the-spot demonstration of the completed experiments and viva voce on the related topics.

Midterm Lab test: 15%.
This evaluation ask for a laboratory test on one of the experiments or on a related experiment which consists of writing code, executing the benchmark program in simulation and analysing the results.

Final Lab test: 25% (Lab test and Presentation).
The final test consist of laboratory test which consists of programing in C/C++ and presentation on the best five experiments of student choice on which student will be examined with viva voce.

Reference:

- David A Patterson, John L. Hennessy, *Computer Architecture: Quantitative Approach*, Morgan Kaufmann, 5^{th} Edition, 2012.
- Trevor E. Carlson, Wim Heirman, Lieven Eeckhout, Ibrahim Hur, Snipper Simulator User Manual, Link: www.snippersim.org
- Todd Austin, Eric Larson, and Dan Ernst, *SimpleScalar: An Infrastructure for Computer System Modeling*, IEEE Computer, Volume 5, Issue 2, 2002.
- VTune Amplifier 2019, https://software.intel.com/en-us/vtune
- SPEC2006/SPEC2017: https://spec.org,
  PARSEC: https://parsec.cs.princeton.edu, and
  SPLASH:https://github.com/SakalisC/Splash-3 benchmarks.