Testing and Verification of VLSI Systems

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18^{th} Jan, 2022

The VLSI Systems: How it Works How it Fails

Human is to error and inefficient!

Broadly, the VLSI systems goes through:

- Specification (Requirements)
- Design
- Manufacturing

Ideally, the end product should be error free!
This really does not happens.

The VLSI Systems: How it works and How it fails

The modern VLSI design is computer based.
(Called as Electronics Design Automation/Computer Aided Design)

Two problems

- The design bugs (Validation and Verification)
- The manufacturing defects (Testing)

Our job is to ensure that the defective or buggy design does not go to the end user.
This is a hard problem to ensure zero defects!

Cases of Failure

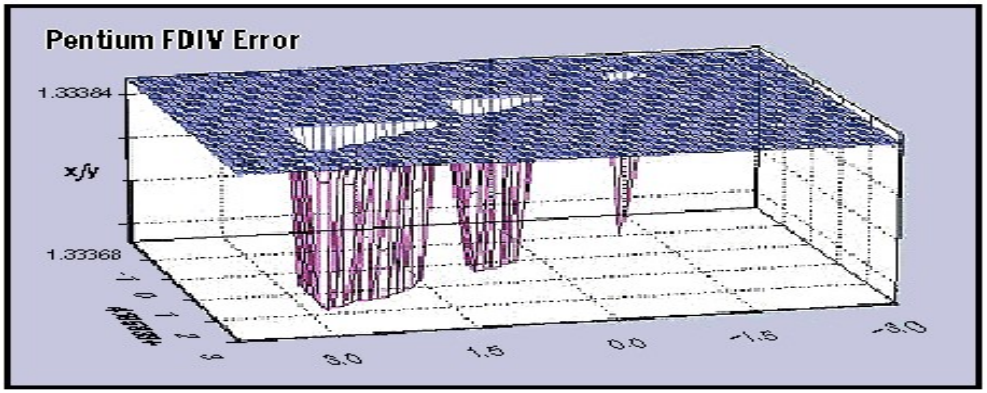

Figure : Bug in floating point unit of Pentium processor

```
Sequence Address  Data       Mnemonic                                  Timestamp
-------------------------------------------------------------------------------
T 524285 000000B2 ----7E--------(-IO-WRITE-)-----------------------------300-ns
  524286 00000018 ----E14C      ( LOCKED MEM READ )                      440 ns
  524287 0000001A F000----      ( LOCKED MEM READ )                      100 ns
```

Figure : F00F bug in processor due to a particular sequence of instructions

Cases of Failure

- Major failure in Space applications (due to software as well as hardware)
- Failures in automobiles (due to software and hardware errors)
- Many failures in IT services such as cloud (hardware and software)

What is our Jobs

- To model the defects
- Specify the functionality
- Design and develop algorithms to test and verify

Course outcome

- to design algorithm
- to use EDA tools
- to be able to diagnose the root cause of failure
- research to explore the newer domain

Lecture Plan

Lecture 1:	Organisational meeting and Introduction to the course
Lecture 2:	VLSI Design flow, Testing process and Test economics
Lecture 3:	Defects, yield analysis and fault modeling
Lecture 4:	Fault equivalence, collapsing and dominance
Lecture 5:	Circuit modeling and true value simulation
Lecture 6:	Serial and parallel fault simulation algorithms

Lecture Plan

Lecture 7:	Deductive and concurrent algorithms
Lecture 8:	Test-detect and differential algorithms
Lecture 9:	Testability measures
Lecture 10:	Combinational ATPG: Algorithms, representation and Redundancy Identification
Lecture 11:	D-calculus and D-algorithm
Lecture 12:	Goel's PODEM Algorithm and Fujiwara's FAN Algorithm

Lecture Plan

Lecture 13:	ATPG system and Test compaction
Lecture 14:	Sequential ATPG for stuck-at fault
Lecture 15:	Design for test (DFT): Serial scan chain architecture
Lecture 16:	Scan architecture with scan compression and compaction
Lecture 17:	Random and Joint-scan architecture
Lecture 18:	Built-in self test (BIST): Architecture and pattern generation (LFSR)

Lectures

Lecture 19:	Response compaction and multiple input signature register (MISR))
Lecture 20:	Memory Testing: failure mechanism and fault modeling
Lecture 21:	Functional RAM and ROM testing
Lecture 22:	Boundary scan standard
Lecture 23:	System test and core based design
Lecture 24:	Simulation based verification

Lectures

Lecture 25:	Basics model checking
Lecture 26:	Formal method of checking: LTL and CTL
Lecture 27:	Formal method of checking: LTL and CTL
Lecture 28:	Combinational equivalence checking
Lecture 29:	Sequential equivalence checking
Lecture 30:	Back-up

Evaluation

Assignment	20%
Midterm:	20%
Mini-project:	25%
Final Test:	35%

Evaluation

- Assignments : Design and implementation of ATPG algorithms and hands-on EDA tools on the benchmark circuits. The implementation would be done using C/C++ only. The assignment will be given on a regular basis as the course progress topic by topic.
- Mini-projects: A list of the projects will be provided by the second week.
- Mid-term: The test will be based on the syllabus covered till the time of Test-2. The format of test paper will be informed prior to the test. The midterm will be conducted during the period of Test-2 (refer Academic calender for Test-2 week)
- Final Test: The final test will cover the entire syllabus however weight will be given more to the untested syllabus.

References and Reading Materials

- Textbook:
  - Bushnell M L and Agrawal V D, Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits, 1st Edition, Springer (2002).
- Reference:
  - Fujita M, Ghosh I and Prasad M, Verification Techniques for System-Level Design, 1st Edition, Morgan Kaufmann (2008).
  - Huth M and Ryan M, Logic in Computer Science, 2nd Edition, Cambridge University Press (2004).
  - Jha N and Gupta S , Testing of Digital System, 1st Edition, Cambridge University Press (2013).
  - Wang L T, Stroud C and Touba N, System-on-Chip Test Architectures: Nanometer Design for Testability, 1st Edition, Morgan Kaufmann (2007).

Question and Discussion

Thank You!