Indian Institute of Technology Tirupati
Computer System Architecture (CS5202)
Quiz 1

Date: 11^{th} Feb, 2019

Registration No.:

Name:

[Max marks: 20][Time: 50 min]

1. According to the trend in device scaling observed by Moore's law, the number of transistor on a chip in 2020 should be how many times the transistor count in 2005? Derive the expression that you use for the calculation, and the answer could be expressed in range. [2 *mark*] [4 *min*]

2. The rate of growth for DRAM capacity has slowed down over the years. For 20 years, DRAM capacity improved by 60% each year. That rate has dropped to around 40% every year and now the improvement is around 25-40% per year. If this trend continues what will be the rate of growth for DRAM capacity by 2025? [2 *mark*] [4 *min*]

3. Calculate the total time a processor might have spent in fetching operands for a program whose statistic of addressing modes usage is given in Figure 1. Assume that at a time only one operand can be fetched either from register or memory. For calculation consider that the processor takes the access time as follow: the register access takes 1 ns, memory access takes 4 ns, and any arithmetic operation needed for address calculation takes 1 ns. [4 *mark*] [8 *min*]

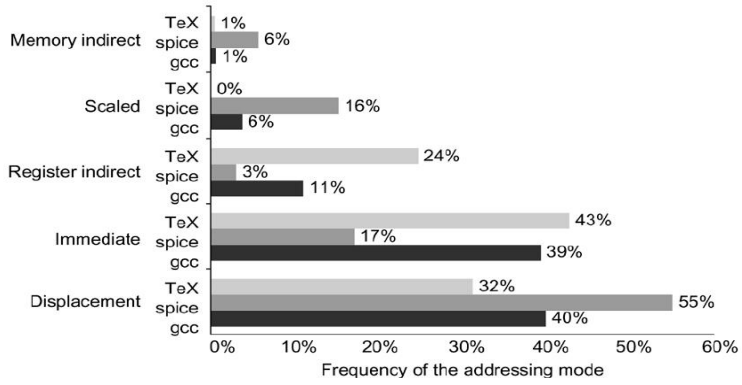

Figure 1: Statistic on usage of addressing modes (reference for Question 3)

4. Explain the different instruction formats the MIPS (MIPS64) architecture uses. The instruction size, opcode, and operands needs to be explained in diagram depicting the size of each field with range of bit-position. [2 *mark*] [4 *min*]

5. Explain the meaning of following instructions in terms of data transfer in micro operations. (The answer to this question should not be expressed in sentence.) [2 *mark*] [4 *min*]

```
LW R3, 100(R2)
DADDU R1, R2, R3
JAL address
ADD.S F1, F2, F3
```

6. Design a data path (with necessary control signal) for updating the program counter (PC) for all the possible instructions in MIPS architecture. The design should be at the level of block diagram, however, where ever necessary show the logic gates. [2 *mark*] [4 *min*]

7. Demonstrate the disadvantage of single-cycle processor design over the multi-cycle design in terms of performance using the following statistics on a program which is executed on these processors. The program is having 50% instructions each takes 1 ns to execute, 30% instructions each takes 2 ns, 15% instruction each take 3 ns and 5% instruction each take 4 ns. [2 *mark*] [4 *min*]

8. For the following instructions which are to be executed in a pipeline processor having five stages answer the following questions:

   (a) Show the progress of execution of each instructions cycle by cycle assuming the ideal pipeline.

   (b) Calculate the total execution time for the ideal pipeline assuming the cycle time as $2ns$.

   (c) Find out the pipeline hazards if any and recalculate the total execution time considering the insertion of NOPs as solution for hazard avoidance.

   ```
   LD R1, 40(R2)
   DADD R5, R1, R7
   DSUB R8, R6, R7
   OR R9, R6, R7
   ```

   [4 *mark*] [8 *min*]