Indian Institute of Technology Tirupati
Computer System Architecture (CS5202)
Problem Set 9.1: Cache performance

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[Points: 20][Time: Two days]

Performance of the cache memory is modelled as follow when the instruction count (IC), memory access per instruction or average memory access (Avg_{access}), miss rate (r_{miss}) and miss penalty (p_{miss}) are given.

$$MEM_{scycle} = N_{miss} \times p_{miss} = (IC \times Avg_{access}) \times r_{miss} \times p_{miss} = (IC \times \frac{access}{instruction}) \times r_{miss} \times p_{miss} \quad (1)$$

where in the above equation MEM_{scycle} is memory stall cycle which is defined as the amount of cycles the processor need to halt for memory to bring the desired data or instruction.

Further, the equation for CPU execution time can be re-expressed as follow:

$$CPU_{time} = CPU_{cycles} \times MEM_{scycle} \times Clk_t \quad (2)$$

The same equations can be extended for the hierarchy of memory system.

1. Derive an equation for MEM_{scycle} considering the following specification of the given computer system. The computer system is having n levels of cache memory: $Level_0$ to $Level_{n-1}$ and a main memory. The *miss rate* and *miss penalty* for each level is different. Further assume that Main memory contains everything ie miss rate is zero and access time of Main memory is equivalent to the miss penalty of $Level_{n-1}$ cache.

2. Supposing we have a processor with CPI = 1.0 (which means a total number of cycle needed to execute an instruction is 1) when all memory accesses hit in the cache. The processor architecture is of RISC type (load-store architecture) and the load and store type instructions total to 50% of the instruction set. If the miss penalty is 25 cycles and the miss rate is 2% and all the access to instruction is hit then how much would be the performance improvement of processor for which all access is hit.

3. Determine the memory stall cycle for processor having the cache memory with miss rate as 30 misses per 1000 memory access (this includes both data and instruction). Consider total instruction count is IC, miss penalty as 25 cycles, and cycle time as t.

4. Given a processor which is having cache memory designed in such a way that it would always perform at the miss rate of 30% irrespective of the type of workloads. Another cache organisation which perform at various miss rates as per the given workload as follow:

workload 1	20%
workload 2	30%
workload 3	15%
workload 4	45%

   Then, compare these two cache organisation on performance and comments why one is better than the other. The remaining parameters are same for both.

5. Assume a CISC type processor architecture where 70% of the instructions access the data memory, let us call them as memory type instruction. Further consider that there are 50% of them which uses memory indirect addressing mode which requires two access to the data memory. Determine the memory stall cycle that the processor see when miss rate is 5% and miss penalty is 10 cycles.