Computer System Design Lab
Design Experiment 5a:
Processor Design

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1 Objective and Problem Statement:

The final outcome of this experiment is the working CPU design consisting consisting of registers, buses, and control signals. This experiment excludes the connection of RAM, ROM, and I/O devices.

In order to design the complete CPU the control and data path for instruction fetch (IF), instruction decode (ID), operand fetch (OF), execution (EX) and write back (WB) need to be designed. The design of CPU system is of *single cycle path.* To check the correctness of the design, the design need to be verified using the test benches.

2 Design and Verification

The following steps are involved in design and verification of the computer system. These steps need to be followed to get the final working computer system.

1. CPU Design: A single cycle data/control path need to be designed for the given Hack ISA. In this step all the paths designed for five different stages need to be connected. In this steps the connection of memory and I/O devices could be avoided.
2. CPU Verification: Once the design is completed, carry out a verification of it. A test bench (.tst) file need to be written and cross checked it against the compare file. **Prepare two test files: one that contains all the possible instructions, and the other containing a small swapping of two number program** and execute it to verify the CPU design.

3 Experimental Flow

1. Write the BHDL code and simulate it using the Hardware simulator.
2. The machine code for all the assembly instruction can be generated using Assembler tool.
3. Prepare the test bench using the generated machine code. Similarly prepare the compare file for each machine instruction.
4. Prepare compare file for program counter (PC), D and A registers.
5. All the address and data bus will be the primary input and output of CPU. These buses will be connected to memory and I/O devices when the full computer system will be designed.

4 Tools:

- Language: The Nand2Tetris HDL and TSL (test scripting language)
  Refer: Appendix A and B of text book.

- Tools: Hardware Simulator of Nand2Tetris.
  `https://www.nand2tetris.org/software`
- Machine and OS: x86_64 machines with any distribution of Linux (Ubuntu or CentOS).

5 Reporting and Evaluation

A report of two pages need to be prepared. The report should have complete CPU data/control path design. The report should describe the function of each component that are part of CPU.

Evaluation will be strictly based on demonstration of the working CPU design. Evaluation consists of design and verification. Score will be assigned for HDL design, .tst files, and .cmp files. Additionally, the students understanding of the design and design methodology will be evaluated as part of oral interaction.