Indian Institute of Technology Tirupati

Computer System Design

Assignment 2

Total points: 100

Closing Date: 11^{th} Oct 2019

Information and Rules:

Assignment 2 gives an option to chose either research or development. The research part of the assignment requires you to carry out a comparative study of two system design methodologies. Whereas, the development part requires you to develop a mini tool.

The assignment could be carried out in a group of two (more than two is not allowed, only one group is allowed to have three members). For a group the contribution of each member must be highlighted. A short interview will be conducted to test the contribution of each member.

Both the assignments, research and development, carry an equal weightage and each requires around 14 to 20 hrs of effective effort.

1 Research

A comparative study between two design methodology and between two processors need to be carried out as part of this assignment. To carry out this study one need to review at least the papers which are listed here in the reading material section.

The following two comparative study need to be carried out:

- Design methodology:
  - The comparison has to be performed between the design methodology used in Rocket chip and Shakti processor.
  - The design methodology comparison should throughly study the reason why such design flow has been adopted. Advantage and disadvantage need to clearly mentioned with some quantitative numbers.
- Processors' feature:
  - Carry out the comparative study between a processor from Rocket chip and from Shakti processor cores.
  - Analyse the advantages and disadvantages of the each of the processor. What are the limitation of these processors? The advantage and disadvantage has to be studied with respect to area, power and performance. A comparison graph for each of these parameters need to be plotted.
  - Identify the applications for which Rocket processor is good at and for which Shakti is good. Explain the reason why they are doing good.
  - Synthesize the netlist of these two processors and program the FPGA and check for the total area these two processor consumes. Gate-level area and timing.
  - Both of these processors are of RISC-V architecture and are open available for experiment.

Tools:

- rc compiler of cadence.

- Modelsim of Mentor.
- Vivado FPGA synthesis tool.
- Some of these tools are available in Electronics Lab (first floor Room #2, Temporary campus)

Reporting:

Prepare a 4 pages report on this. The format of the report needs to be strictly as the given format in IEEE double column format.

2 Development

Design and development of high-level language and corresponding synthesis tool for BHDL. The synthesis tool would take the program written in the language that you have designed and it would produce a output file contain the hardware design at gate level netlist.

Use C/C++ to code to design the synthesis tool. The language should have the following features:

- Basic features:
  - Support the module definition such as CHIP ¡chipname¿
  - Should support port declaration
  - Should support interconnect declaration
  - Should support multibit bus declaration
  - Should support if-else statement for Multiplexor
  - Should support adder and subtracter, for example: if I write a + b then it should give me an full adder design in my output file.
- Additional features:

  I will send you the advance feature in next email.

The feature of synthesis tool: The synthesis tool should perform the two important task. One is to perform the syntax check and the next one is to generate the translate the high-level description to gate level netlist.

An user manual for the tool need to be prepared explaining the feature of your high level language, different errors the synthesis tool can handle.

Example:

```
CHIP myChip {
     // port and interconnect declaration
     input myinput_port1, myinput_port2 ;
     input myselect ;
     output myoutput_port1 ;

     if (myselect = 0) then
        myoutput_port1 <= myinput_port1 ;
     elseif (myselect = 1) then
        myoutput_port1 <= myinput_port2 ;
}
```

The synthesized output file of the above highlevel HDL should look like the following.

```
CHIP myChip{
    IN myin_port1, myin_port2;
    OUT myoutput_port1;

    INV(in1 = myselect, out=net1 )
    AND(in1 = myin_port1, in2 = net1, out = net2 );
    AND(in1 = myin_port2, in2 = myselect, out = net3);
    OR(in1 = net2, in2 = net3, out = myout_port1);
}
```

Reading Materials:

- Shaki Processor: https://shakti.org.in
- RISC-V: www.riscv.org
- Open source hardware challenges, by Prof. Karu Sankara Lingam, University of Wisconsin.
- UC Berkely RISC-V research group
- Model Sim design synthesis tool.