Indian Institute of Technology Tirupati

Computer System Design

Assignment 1

Total points: 100

Closing Date: 30^{th} August 2019

Rules:

Rule 1: Solve 1, 2, 3, and any one from 4 and 5.

Rule 2: The references from Wikipedia, or any other social media site is not acceptable. References should be either from text book or from reputed journals or conference proceedings. Anything that is not referred will be accepted as your knowledge gained from experience.

Rule 3: The assignment should be submitted in pdf file. The figures could be hand-drawn image file appropriately placed in the report with caption. The figures and tables should have caption and number.

Exercises:

1. Explain about the main components of computer hardware system? Depict using a block diagram the connection and interaction of these components. [*points* : 10]

2. What do you understand by CISC and RISC? Give at least four example of processors and their application domain, which are designed based on either of these two ideas. Provide your comment on why a particular application choses RISC or CISC type of processor? Provide appropriate references wherever needed. [*points* : 30]

3. Explain the basic concept of MIMD (multiple instruction multiple data), SIMD (single instruction multiple data), SISD (single instruction single data), and MISD (multiple instruction single data) computing concept. For each type of concept give appropriate examples to explain the basic working principle. [*points* : 20]

4. Design an SoC (system-on-chip) which is going to be used in the next generation smart phone. The next generation smart phone would have the following features. [*points* : 40]

   (a) Central processing unit: Processing core 1 and Processing core 2.

   (b) Graphics (image and video): graphics core 1.

   (c) ML Accelerator: a dedicated processing unit for machine learning.

   (d) A core for encryption and decryption: crypto core 1

   (e) Cores for communication: communication core (COM) and digital signal processing core (DSP)

   (f) The cores are interconnected via on-chip network and buses.

   (g) Assume there are dedicated cache memory for each of the core and a shared on-chip cache memory which would serve all the cores as requested. Apart from the cache memory the system also have RAM as main memory and a flash drive as storage.

   The design should clearly explain the reason for connecting one core with another. The size of buses should be specified (example: as 16 bit, 32 bit or 64 bit). You have to decide your own network topology. Function of each core should be clearly explained. Give one example application and explain how that application is going to use all of these cores, network, and memory as it goes for execution. Explain this step by step. Wherever necessary assume additional components such as I/O devices (camera, sensor etc.) or any other core.

5. Design a next generation general purpose computer (processor system) which will have the following requirement and specification. [*points* : 40]

   (a) The system will have multiple system cores: processor core 1, processor core 2, processor core 3, and processor core 4. Each core can be of different size.

   (b) There will be processor cores for graphics (image and video): graphics processing core 1, graphics processing core 2, ... and graphics processing core 6.

(c) There will be one co-processor for scientific computation.

(d) there will be a hardware accelerator for document processing: document processor 1 and document processor 2.

(e) The system will have on chip cache memories for data and instruction separately each of the system cores. Other cores will have their own dedicated level 1 cache memory. Apart from the dedicated cache memories the system will have off-chip level 2 and level 3 caches and a RAM main memory.

(f) Each of the processing core are interconnected via an on-chip network and buses with the other components such as memory and I/O devices.

The design should be neatly drawn with label for each of the cores, block, and module and proper directions for each of the signal and buses. The detail functionality of each core or module should be explained. The reason for each connection should be clear described. The size of data and address bus need to be mentioned. The network topology need to be decided. Give example applications (which are typically executed on desktop or workstation computer) to demonstrate how the applications make use of each of the cores, memory, on-chip network, and buses. The demonstration should be explained step by step.

Reading Materials:

- Chapter 1, Computer System Design: System-on-Chip, First Edition. Michael J. Flynn and Wayne Luk.
- ARM Cortex-M for Beginners: An overview of the ARM Cortex-M processor family and comparison, Joseph Yiu, March 2017.
- Enabling the Next Mobile Computing Revolution with Highly Integrated ARMv8-A based SoCs, White paper by ARM and Qualcomm.
- Snapdragon S4 Processors: System on Chip Solutions for a New Mobile Age, A White Paper from Qualcomm, 2011.
- Introduction to Intel Architecture: The Basics, Jim Turley, Intel. `https://www.intel.com/content/dam/www/public/us/en/documents/white-papers/ia-introduction-basics-paper.pdf`