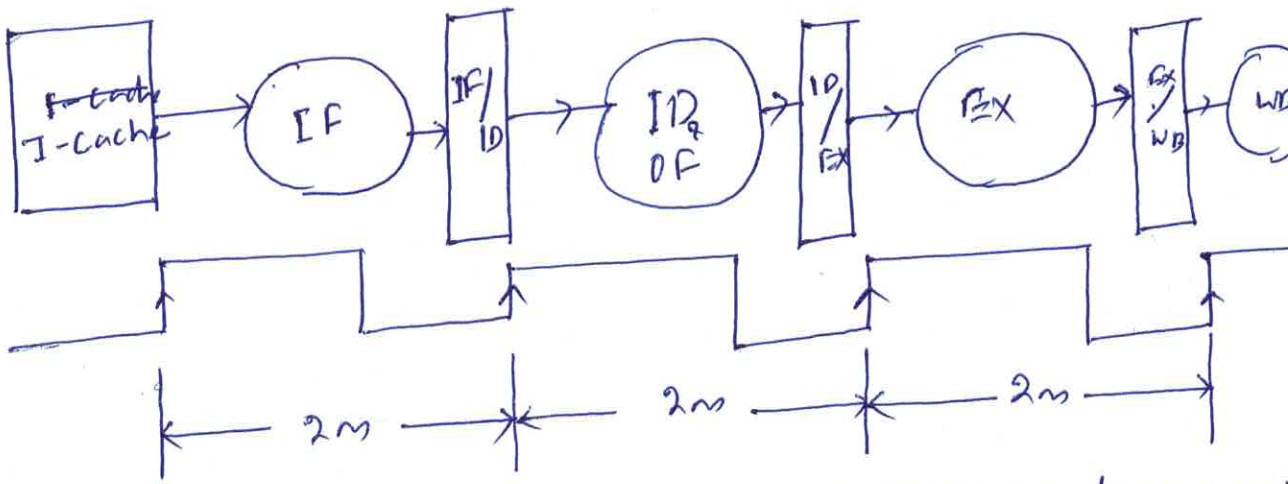
- Super Scalar Architecture -

- How to go beyond the pipeline throughput- limit?

Two things come in mind -

- deepening the pipelining stages
- widening the pipelines

Deepening the pipeline stages :-



In reality all the stages does not take exact the same clock cycle time.

The real scenario could be :-

4-Stages
- IF - 2ns
- ID - 1ns
- EX - 1.5ns
- WB - 1ns

Five stages
- IF - 2ns
- ID - 0.5ns
- OF - 0.5ns
- EX - 1.5ns
- WB - 2ns

not much time: IF, ID

IF	IS	ID	EX	DF	DS	TC	WB
①	②	③	④	⑤	⑥	⑦	⑧
1ns	1ns	1ns	1ns	1ns	1ns	1ns	1ns

RS4000 processor

→ The modern high performance processor uses 10-14 stages of pipeline.

→ Danger of having more than 14-stages pipeline?

Widening the pipeline ~~stages~~ :-

- Assumption :- Everything is good (ideal pipeline)