Lecture - 7 | Sept 3, 2019

- D-FF design
  - Behavioral code
  - Simulation Methodology
  - comparison table
- 1-bit Register :-
- N-bit Register :-
- shift-register :-
  - left shift-register
  - Right shift-register
- counter :-
  - up-down counter
- program counter (PC)
  - PC ← PC+1
  - PC ← PC+2
  - PC ← PC+4

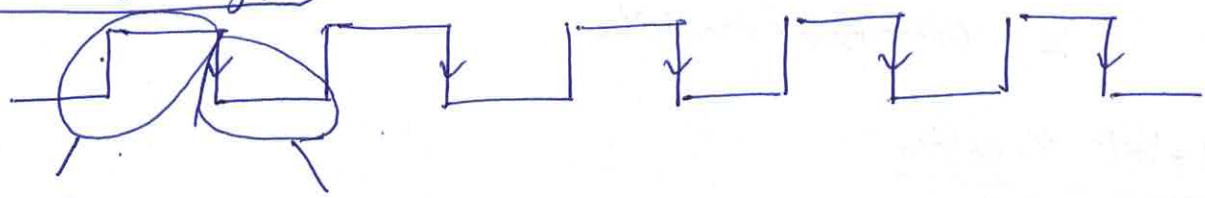
(2)

- BHDL code ✓

- Simulation :-

The concept of clock pulses :-

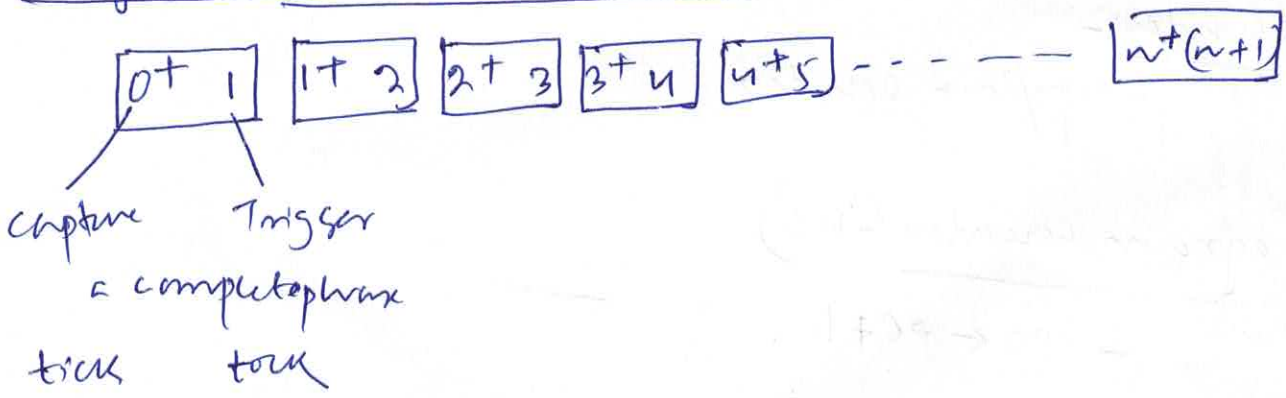
Negative edge triggers :-



Capture phase (The input at D input will be sampled to Master Latch)

Trigger phase (The sampled input will be effective at the Q-output)

- progress of time in Simulation :-



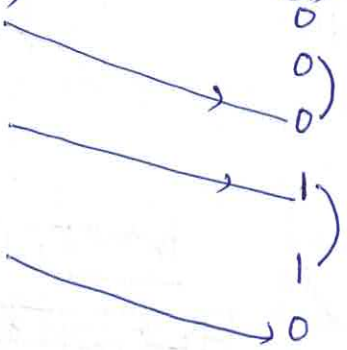
Similarly for the positive edge triggered clock :-

Do it by yourself.

Comparison file (.cmp) :-

Three parameters :- ① Time
② Inputs
② out-puts

Time	inputs (D)	output (Q)
0+	0	0
1	0	0
1+	1	0
2	1	1
2+	0	1
3	0	0
3+		
4		
4+		



Example chip using inbuilt DFF :-

```
CHIP DFF {

    IN D;
    OUT Q;
    BUILTIN DFF;
    CLOCKED D, Q;   // Explicit clocking specification
                       for simulation.
}
```

(4) **1-bit Register :-**

functional specification :- To be able to write & read 1-bit data.

- ~~To store load one-bit of information~~

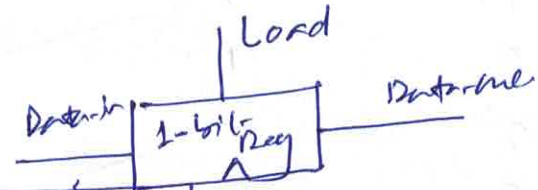
~~Two main function:~~
- Read (output)
- Write (Load)

inputs :- ① Data-in 1 bit,
② Load control signal

outputs :- Data-out 1 bit

Function :- if

Diagram :-



Internal Design :-

Note - ① in this design the clock signal is implicit
② This design to be ~~[illegible]~~ built using the inbuilt DFF.

Code :-

```
~~CHIP my1bit {
    IN Data, Load;
    OUT Dout;
    PARTS:
    DFF(Din = Din, Q = Dout)~~
```

8-bit Register :-

functional specifications :-

~~To load 8-bit of ~~and inp~~ data input~~

To be able to read & write 8-bit of data.

input :-

output :-

function :-

Diagram :-

Code :-

Shift Register :-

A register capable of read, write, and shift operation

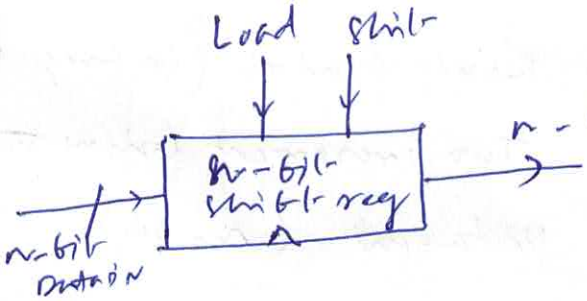
Inputs :- ① Data in (n-bit)
② Load control signal (1-bit)
③ Shift control signal (1-bit)

Outputs :- ① Data-out (n-bit)

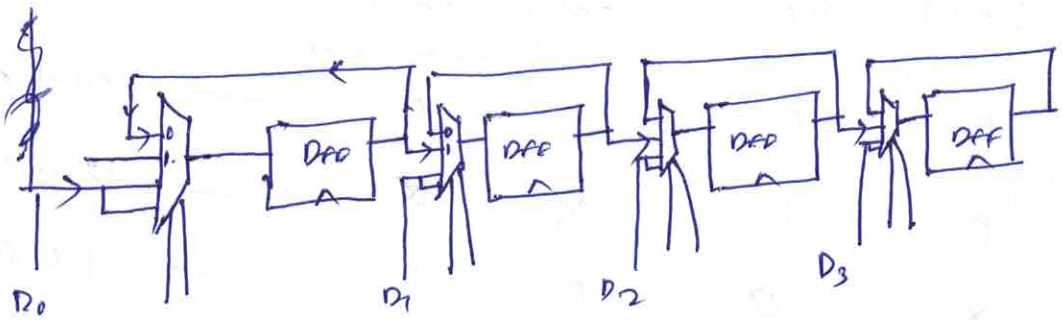
Function :-

Load	Shift	
1	0	→ Load Data in to Register
0	1	→ Perform shift
1	1	→ Perform Load
0	0	→ ~~Keep~~ Retain the Data

Block Diagram :-



Design of ~~4-bit~~ Right shift Register :-



(6)

Counter :-

A sequence counter with up & down control signal.

Program Counter :-

A special kind of counter used for fetching instruction

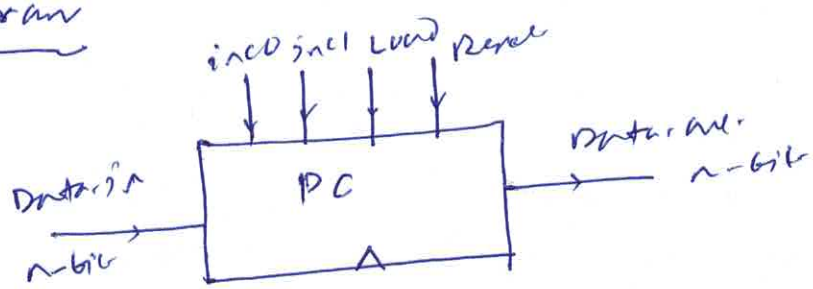
inputs :- (1) Data-in (n-bit)
(2) Load control signal
(3) Reset control (to bring PC to zero)
(4) Two increment control signals.

outputs :- Data-out (n-bit)

function :-

Load	Reset	inc0	inc1	
1	0	0	0	→ Load new data
0	1	X	X	→ Reset to zero
X	0	0	1	→ PC ← PC+1
X	0	1	0	→ PC ← PC+2
X	0	1	1	→ PC ← PC+4
0	0	0	0	→ Retain Data

Block diagram



Design :-