

- Last Lecture -

- Basic digital gates
- Combinational logic block
 - Multiplexer
 - DeMultiplexer
 - Decoder
 - ↓ Encoder
- Multibit-Multibit logic
- Hardware description language (VHDL)
- Test bench writing (TSL)
 - * Simulation

- Today's Lecture :-

- Objective - Designing an Arithmetic & Logic Unit
- Data representation
- Basic arithmetic operations
 - Addition
 - Subtraction

Combinational Logic for arithmetic operation

- Half adder
- Full adder
- ~ n-bit adder & subtractor

Arithmetic & Logic Unit -

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Data representation :-

The number system: -



Integer :- Decimal number system (base = 10)

Octal number system (base = 8)

Hexadecimal system (base = 16)

A number can be represented as:

$$\begin{aligned}
 & a_4 \ 3 \ 2 \ 1 \ 0 \\
 a_4 a_3 a_2 a_1 a_0 &= +10^4 \times a_4 + 10^3 \times a_3 + 10^2 \times a_2 + 10^1 \times a_1 \\
 &= 10^4 \times a_4 + 10^3 \times a_3 + 10^2 \times a_2 + 10^1 \times a_1 \\
 &\quad + 10^0 \times a_0 \\
 \text{if } a_i &\in \{0, 1, 2, 3, 4, 5, 6, 7, 8, 9\}
 \end{aligned}$$

Call it as decimal system

where base is 10

$$a_0 = 2$$

$$a_1 = 1$$

$$a_2 = 4$$

$$a_3 = 0$$

$$a_4 = 8$$

$$\begin{array}{r}
 a_4 \ a_3 \ a_2 \ a_1 \ a_0 \\
 \hline
 8 \ 0 \ 4 \ 1 \ 2
 \end{array}$$

$$\begin{aligned}
 &= [10^4 \times 8 + 10^3 \times 0 + 10^2 \times 4 + 10^1 \times 1 \\
 &\quad + 10^0 \times 2]
 \end{aligned}$$

$$= 10^4 \times a_4 + 10^3 \times a_3 + 10^2 \times a_2 + 10^1 \times a_1$$

$$+ 10^0 \times a_0$$

$$= \sum_{i=0}^n b^i a_i \rightarrow \text{nr of digits no.}$$

For binary system

$$\boxed{b = 2 \text{ and } a_i \in \{0, 1\}}$$

+ve & -ve integer number in binary system

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Example :-

3 bit number system

<u>a₂a₁a₀</u>	<u>Mag</u>	<u>2' comp</u>
0 0 0	0	0
0 0 1	1	+1
0 1 0	2	+2
0 1 1	3	+3
1 0 0	4	-4
1 0 1	5	-3
1 1 0	6	-2
1 1 1	7	-1
<u>1000</u>	<u>-8</u>	

$$(+a) + (-a) = 0$$

$$1 + 2 = 8$$

$$2 + 6 = 8$$

$$3 + 5 = 8$$

$$4 + 4 = 8$$

General form =

$$2^n - a = -a$$

in 2' complement

How to generate 2' complement - number :-

$$\begin{array}{r} 1.0.00 \\ - 0.1.0 \\ \hline 110 \end{array} \quad -2$$

Easy way

One's complement + 1

$$0.1.0$$

$$\rightarrow 1.0.1$$

$$\begin{array}{r} 110 \\ \hline -2 \end{array}$$

$$0.0.1$$

$$\begin{array}{r} 1' \rightarrow 110 \\ + 1 \rightarrow \hline 111 \end{array} \quad -1$$

Overflow & largest possible number :-

Example $\xrightarrow{3\text{-bit}} [-1 \text{ to } 3]$

Example $\xrightarrow{4\text{-bit}} [-8 \text{ to } 2]$

General $\xrightarrow{n\text{-bit}} [2^{(n-1)} \text{ to } 2^{(n-1)} - 1]$

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An arithmetic operation :-

- Addition (+)
- Subtraction (-)

Example (Adding two bits)

Example (Adding three bits)

Combinational cir-

Half adder

Combinational cir-

- Full adder
- Using XOR gates
- Full adder using half adder

Example - n-bit number

$$[-5 + (+2) = +7] \rightarrow \text{required } 4 \text{ bit sum}$$

$$\begin{array}{r}
 & 0101 \quad - +5 \\
 + & 0010 \quad - +2 \\
 \hline
 & 0111 \quad \rightarrow +7
 \end{array}$$

Designing a circuit

